

CLAIMS

What is claimed is:

- 1 1. An input circuit for an RF power amplifier comprising:
2 an input network having a transformer with a primary side and a secondary side, wherein
3 an RF input signal is coupled to the primary side;
4 a limiting amplifier having an input coupled to the secondary side of the transformer and
5 an output for providing an input to the RF power amplifier; and
6 a DC feedback loop coupled to the limiting amplifier.
- 1 2. The input circuit of claim 1, wherein the limiting amplifier is comprised of a
2 plurality of inverters connected in series between the limiting amplifier input and the
3 limiting amplifier output.
- 1 3. The input circuit of claim 2, further comprising an amplifying stage coupled
2 between the input of the limiting amplifier and the transformer.
- 1 4. The input circuit of claim 1, further comprising an amplifying stage coupled
2 between the input of the limiting amplifier and the transformer.
- 1 5. The input circuit of claim 4, wherein the amplifying stage is comprised of a
2 common-source amplifier.

- 1 6. The input circuit of claim 4, wherein the amplifying stage is comprised of a
2 common-gate amplifier having one or more switching devices.
- 1 7. The input circuit of claim 6, wherein a bias is provided to a gate terminal of each
2 of the one ore more switching devices.
- 1 8. The input circuit of claim 7, wherein the bias is a DC bias.
- 1 9. The input circuit of claim 6, wherein a dynamic bias is provided to the gates of
2 the switching devices.
- 1 10. The input circuit of claim 6, wherein the RF input signal is coupled to both the
2 source and gate of one or more of the switching devices of the amplifier stage.
- 1 11. The input circuit of claim 6, wherein the common gate amplifier has two
2 switching devices, and wherein the RF input signal is coupled to both the source and the
3 gate of each of the two switching devices.
- 1 12. The input circuit of claim 1, wherein the RF power amplifier is formed on a
2 semiconductor substrate, and wherein the input circuit is formed on the same
3 semiconductor substrate.
- 1 13. The input circuit of claim 12, wherein the semiconductor is a complementary
2 metal oxide semi-conductor (CMOS) semiconductor.

1 14. A predriver circuit for an RF power amplifier comprising:
2 an input circuit coupled to an RF input signal; and
3 a plurality of inverters coupled in series between the input circuit and an input of
4 the RF power amplifier.

1 15. The predriver circuit of claim 14, further comprising an amplifying stage coupled
2 between the plurality of inverters and the input circuit.

1 16. The predriver circuit of claim 14, wherein the amplifying stage is comprised of a
2 common-source amplifier.

1 17. The predriver circuit of claim 14, wherein the amplifying stage is comprised of a
2 common-gate amplifier having one or more switching devices.

1 18. The predriver circuit of claim 17, wherein a bias is provided to the gates of the
2 switching devices.

1 19. The predriver circuit of claim 18, wherein the bias is derived from the output of
2 the RF power amplifier.

1 20. The predriver circuit of claim 18, wherein the bias is derived from both the input
2 and the output of the RF power amplifier.

1 21. The predriver circuit of claim 18, wherein the bias is set to cause the DC bias
2 levels of the input and the output of the RF power amplifier to be approximately equal.

1 22. The predriver circuit of claim 14, wherein the inverters are CMOS inverters.

1 23. A method of controlling a power amplifier having a predriver circuit comprising:
2 sensing the input and output DC levels of the power amplifier;
3 comparing the sensed DC levels;
4 creating a feedback signal based on the difference between the sensed DC levels; and
5 adjusting the DC bias levels in the predriver so that the input and output DC levels of the
6 power amplifier are maintained in a predetermined relationship.

1 24. The method of claim 23, wherein the feedback signal is a negative feedback
2 signal.

1 25. The method of claim 23, wherein the DC bias levels in the predriver are adjusted
2 so that the input and output DC levels of the inverting power amplifier are approximately
3 equal.

1 26. The method of claim 23, wherein the power amplifier is an inverting power
2 amplifier.

1 27. An amplifier comprising:

2 a transformer having a primary side and a secondary side, the secondary side having first
3 and second terminals, wherein the primary side is adapted to receive an input
4 signal;
5 a first switching device having first and second nodes, the first node coupled to the first
6 terminal of the secondary side of the transformer;
7 a second switching device having third and fourth nodes, the third node coupled to the
8 second terminal of the secondary side of the transformer;
9 a first capacitance coupled between the second node of the first switching device and the
10 third node of the second switching device; and
11 a second capacitance coupled between the first node of the first switching device and the
12 fourth node of the second switching device.

1 28. The amplifier of claim 27, wherein the first and third nodes are source nodes of
2 the switching devices.

1 29. The amplifier of claim 28, wherein the second and fourth nodes are gate nodes of
2 the switching devices.

1 30. The amplifier of claim 27, wherein the input signal is an RF input signal.

1 31. The amplifier of claim 27, further comprising a current path for allowing DC
2 current to flow through the first and second switching devices.

1 32. The amplifier of claim 31, wherein the current path is provided by coupling a
2 voltage reference node through a center tap formed in the transformer.

1 33. The amplifier of claim 31, wherein the current path is provided by one or more
2 inductors coupled between the first and third nodes of the switching devices and a voltage
3 reference node.